	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	48	(gate near dielectric) near15 (thickness) near15 (oxid$4) near15 (temperature)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/24 19:34	
2	BRS	L2	0	(gate near dielectric) near15 (top) near15 (oxid$4) near15 (temperature)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/24 19:35	
3	BRS	L3	186	(gate near dielectric) near15 (top) near15 (oxid$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/24 19:37	
4	BRS	L4	10	(gate near (thickness) near10 (top) near15 (oxid$4)	USPAT; US-PGPUB; JPO; DERWENT; IBM_TDB	4 19:37	

	U	1	Document ID	Title	Current OR	Pages	Issue Date
1	☐	☐	US 6448126 B1	Method of forming an embedded memory	438/216	20	20020910
2	☐	☐	US 6346275 B1	DRAM cell with vertical CMOS transistor	438/386	5	20011201
3	☐	☐	US 6303454 B1	Process for a snap-back flash EEPROM cell	438/305	13	20011016
4	☐	☐	US 6211551 A	Dram cell with three-sided-gate transfer device	257/296	22	20000919
5	☐	☐	US 5978272 A	Nonvolatile memory structure for programmable logic devices	365/185.27	12	19991102
6	☐	☐	US 5960289	Method for making a dual-thickness gate oxide layer using a region	438/275	12	19990928
7	☐	☐	US 5828605 A	Snapback reduces the electron and hole trapping in the tunneling oxide of flash EEPROM	365/185.29	11	19981027
8	☐	☐	US 5726933 A	Clipped sine shaped waveform to reduce the cycling-induced electron trapping in the tunneling oxide of flash EEPROM	365/185.18	11	19960310

	U	1	Document ID	Title	Current OR	Pages	Issue Date
9	☐	☐	US 5567270 A	Process of forming contacts and vias having tapered sidewall	438/701	19	19961022
10	☐	☐	US 5485423 A	Method for eliminating of cycling-induced electron trapping in the tunneling oxide of 5 volt only flash EEPROMS	365/185.19	8	19960116
11	☐	☐	US 5481494 A	Method for tightening VT distribution of 5 volt-only flash EEPROMS	365/185.24	9	19960102
12	☐	☐	US 4722912 A	Method of forming a semiconductor structure	438/595	5	19880202
13	☐	☐	US 4658495 A	Method of forming a semiconductor structure	438/585	7	19870421
14	☐	☐	US 3627589 A	METHOD OF STABILIZING SEMICONDUCTOR DEVICES	438/143	6	19711214

	U	1	Document ID	Title	Current OR	Pages	Issue Date
15	☐	☐	US 4466172 A	FET contg. device mfr. - having self registering source and drain contacts and gate electrodes connected to interconnect lines		13	19840821